UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,498	05/29/2001	Tetsuo Morita	209174US2	3173

22850 7590 03/26/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
KUMAR, SRILAKSHMI K

ART UNIT	PAPER NUMBER
2675	4

DATE MAILED: 03/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/865,498	Applicant(s) MORITA, TETSUO	
	Examiner Srilakshmi K. Kumar	Art Unit 2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al (US 6,411,273).

As to independent claim 1, Nakamura et al disclose a liquid crystal display comprising; a pixel array portion having signal lines and scanning lines horizontally and vertically aligned, and pixel transistors formed in the vicinity of each intersection of said signal line and said scanning line (col. 34, lines 5-8, 13-22); a plurality of first latch circuits configured to latch digital gradation data consisting of a plurality of bits in different timings (Fig. 9, item 102, col. 41, lines 44-col. 42, line 17); a plurality of second latch circuits which are provided in accordance with each of a plurality of said first latch circuits and latch data latched by each of a plurality of said first latch circuits at the same time (Fig. 9, items 103, col. 41 lines 44-col. 42, line 17); a plurality of D/A converters (Fig. 9, item 104); a signal line selection circuit configured to switch whether said analog gradation voltage is supplied to each signal line so that said signal lines in said pixel array portion are driven every multiple signal lines in multiple times (col. 42 line 51-col. 43, line 24).

As to dependent claim 2, limitations of claim 1, and further comprising, wherein said signal line selection circuit has a plurality of analog switches, which are provided in accordance with each of said signal lines and switch whether said analog gradation voltage is supplied to corresponding signal line (col. 42, line 51-col. 43, line 24); said signal line selection circuit controls a plurality of said analog switches to be turned on/off so that said signal lines are drive every multiple signal lines in multiple times (col. 42, line 51-col. 43, line 24).

As to dependent claim 3, limitations of claim 2, and further comprising, wherein said first latch circuits, said second latch circuits, said D/A converters and said analog switches are formed on the same insulating substrate as said signals, said scanning lines and said pixel transistor (col. 34, lines 13-34); a plurality of said analog switches are provided in accordance with each of said D/A converters and a plurality of said analog switches are sequentially turned on one by one (col. 42, line 51-col. 43, line 23).

As to dependent claim 4, limitations of claim 2, and further comprising, wherein the number of signal lines is n (n is an integer not less than 2), n/m sets of said first latch circuits, said second latch circuits and said D/A converters are provided and m pieces of analog switches are provided for each of said D/A converters (Fig. 9, col. 41, lines 44-col. 42, line 17).

As to dependent claim 5, limitations of claim 4, and further comprising, wherein said first latch circuit includes a digital gradation data for said first latch circuit (col. 41, line 44-col. 42, line 17).

As to dependent claim 6, limitations of claim 1, wherein said first latch circuit includes a first level conversion circuit conversion circuit configured to convert digital gradation data into

digital gradation data in a first voltage range (col. 41, lines 44-col. 42, lines 17, col. 42, line 51-col. 43, line 23).

As to dependent claim 7, limitations of claim 1, and further comprising, comprising a second level conversion circuit which is inserted between said second latch circuit and said D/A converter (col. 41, lines 8-63).

As to dependent claim 8, limitations of claim 1, and further comprising, wherein said D/A converter includes a decoder configured to decode an output from said second latch circuit (col. 42, line 51-col. 43, line 17); and a plurality of analog switches which are controlled to be turned on/off in accordance with a decoding result by said decoder (col. 42, line 51-col. 43, line 17, col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 9, limitations of claim 1, and further comprising, wherein said D/A converter includes a plurality of resistance devices connected between a first voltage terminal and a second voltage terminal in series (col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 10, limitations of claim 9, and further comprising, a plurality of electric current amplification circuits connected to said respective connection points of a plurality of said resistance devices, wherein selection circuit selects any one of outputs from said electric current amplification circuits based on an output from said second latch circuit (col. 45, lines 6-52, col. 46, lines 10-57).

As to dependent claim 11, limitations of claim 1, further comprising a shift register configured to output a latch timing signal of each of a plurality of said first latch circuits (Fig. 9, col. 34, lines 5-8, 13-22), wherein a plurality of said second latch circuits carry out the latch

operation based on a load signal generated by an output from said shift register (Fig. 9, col. 34, lines 5-8, 13-22).

As to dependent claim 12, limitations of claim 12, limitations of claim 1, and further comprising, wherein said signal line selection circuit selects all signal lines corresponding to either odd numbered pixels or even numbered pixels in a first have of one horizontal line display period, and selects all signal lines corresponding to the other of odd numbered pixels or even numbered pixels in a last half of one horizontal line display period (col. 34, lines 5-55).

As to dependent claim 13, see claim1, above.

3. Claims 14-19 rejected under 35 U.S.C. 102(e) as being anticipated by Kimura (US 6,281,826).

As to independent claim 14, Kimura discloses a voltage generating apparatus, including a data latch circuit (Fig. 7a, items 400 and 500), wherein the data latch circuit comprises; a memory circuit which has first and second inverters having one output terminal connected to the other input terminal and the other output terminal connected to one input terminal and stores therein digital data (Fig. 7a, col. 25, lines 43-67); first and second switch devices configured to switch and controlling whether a power supply voltage is supplied to said first and second inverters and a third switch device configured to switch and controlling whether said digital data is inputted to said memory circuit (col. 25, lines 43-67, col. 26, lines 30-59); an output circuit configured to read digital data stored in said memory circuit and having a passing electric current prevention function so as not to cause a passing electric current to flow from a power supply terminal of said output terminal to a ground terminal in said sampling period (col. 25, lines 43-67, col. 26, lines 30-59, col. 28, lines 20-59); said first and second switch devices being turned

on in a period other than a cyclic sampling period to supply a power supply voltage to said first and second inverters and said third switch device being turned on in said sampling period to input digital data to said memory circuit (col. 25, lines 43-67, col. 26, lines 30-59, col. 28, lines 20-59).

As to dependent claim 15, limitations of claim 14, and further comprising, wherein said output circuit outputs a signal having predetermined logic in said sampling period, and inverts and outputs data stored in said memory circuit in a period other than said sampling period (col. 25, lines 43-67, col. 26, lines 30-59, col. 28, lines 20-59).

As to dependent claims 16 and 18, limitations of claim 15, and further comprising, wherein said output circuit includes first and second logic operation circuits which outputs a signal having a predetermined logic in said sampling period and inverts and outputs an output from said first and second inverters in a period other than said sampling period (col. 25, lines 43-67, col. 26, lines 30-59, col. 28, lines 20-59).

As to dependent claims 17 and 19, limitations of claims 16 and 18, and further comprising, wherein said first and second logic operation circuits include any one of a NAND gate, NOR gate and a clocked inverter (col. 25, lines 43-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (US 6,411,273) in view of Kimura (US 6,281,826).

As to independent claim 20, see limitations of claims 1 and 14, above. It would have been obvious to one of ordinary skill in the art to combine Nakamura et al with that of Kimura as Nakamura et al disclose an active matrix liquid crystal display apparatus comprising data latch circuits and D/A converters. Kimura discloses the circuitry of the data latch circuits and the D/A converters. Thus, Nakamura et al is combinable with Kimura.

As to dependent claim 21, limitations of claim 20, see limitations of claim 16, above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Srilakshmi K. Kumar** whose telephone number is **(703) 306 5575**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703 305 9720. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872 9314 for regular communications and 703 308 9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 4700.

Srilakshmi K. Kumar
Examiner
Art Unit 2675

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

SKK
March 21, 2003